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FIG. 1A

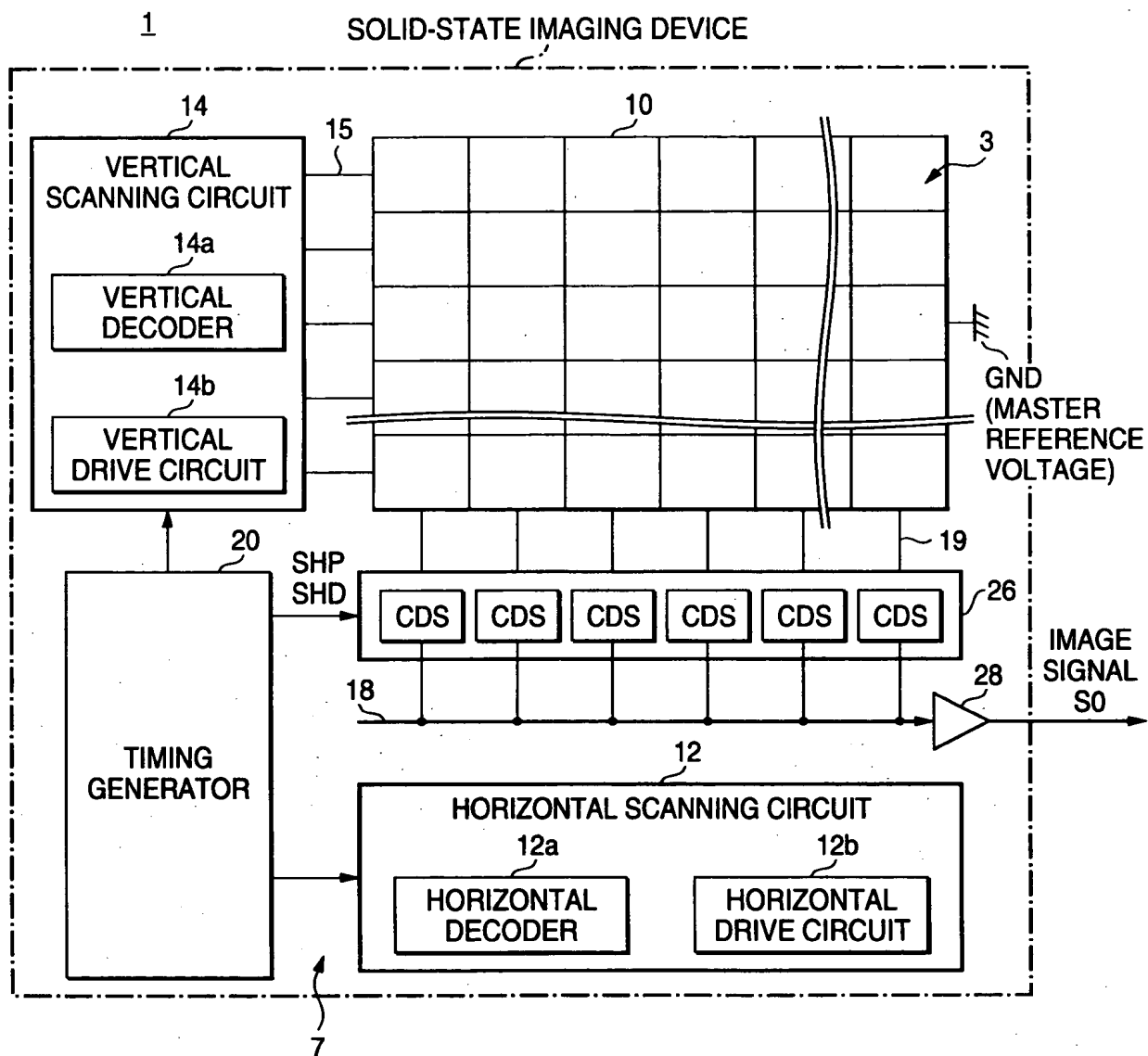
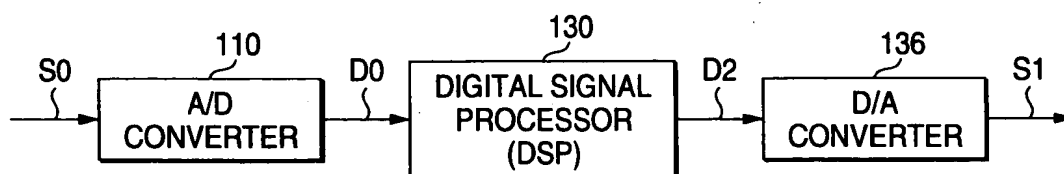


FIG. 1B



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FIG. 2A

*DEVICE STRUCTURE {

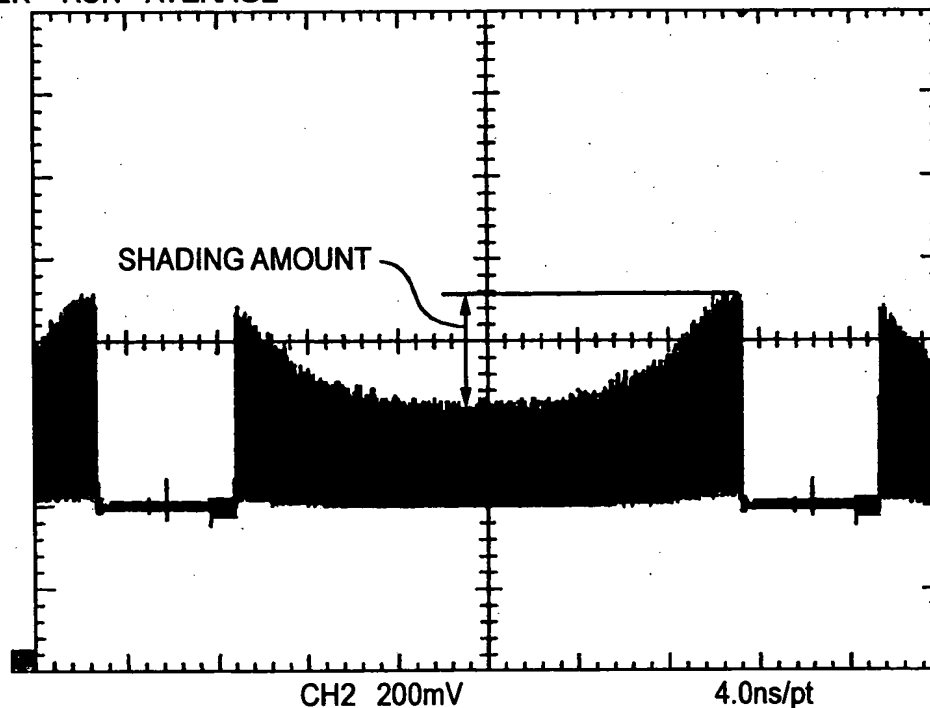
- VGA-COMPATIBLE CMOS SENSOR (APPROX. 0.3 MILLION PIXELS)
- CLOCK FREQUENCY: 6MHz (FRAME RATE 13.3fps)
- UNIT PIXEL IN 3-TRANSISTOR STRUCTURE
- PIXEL PITCH 4.1 μ m

*DRIVE CONDITION {

- POWER VOLTAGE 3.0V
- TRANSFER GATE DRIVE VOLTAGE HAVING VARIABLE LOW LEVEL
- OTHER DRIVING TO THE PIXEL BY 0V AND POWER VOLTAGE (3.0V)

FIG. 2B

TEK RUN AVERAGE

M: 20.0 μ s 250MS/s

A: CH4/1.64V

B: CH3/1.57v

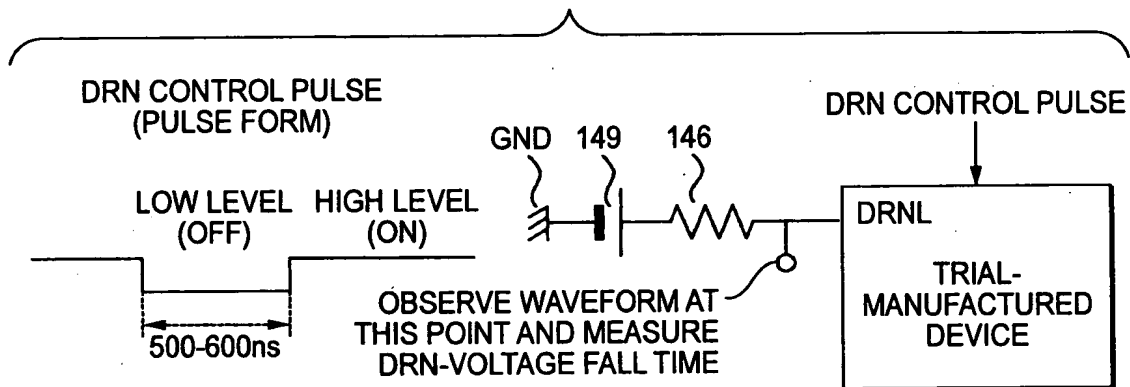
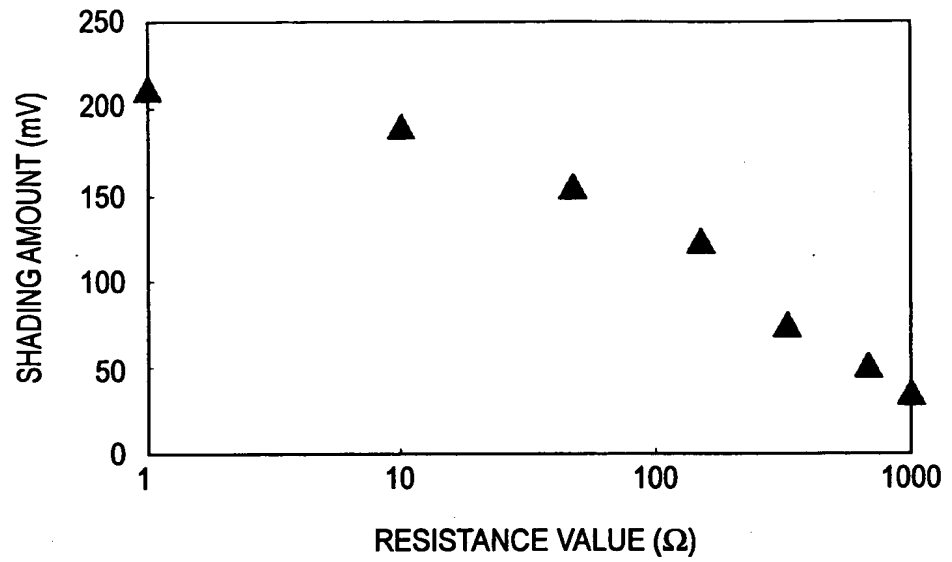
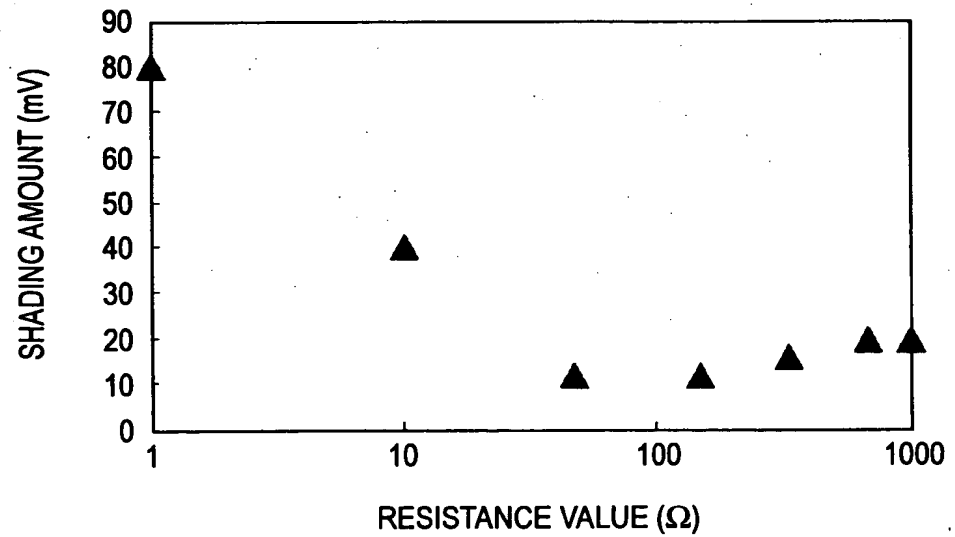
FIG. 3

FIG. 4A**FIG. 4B**

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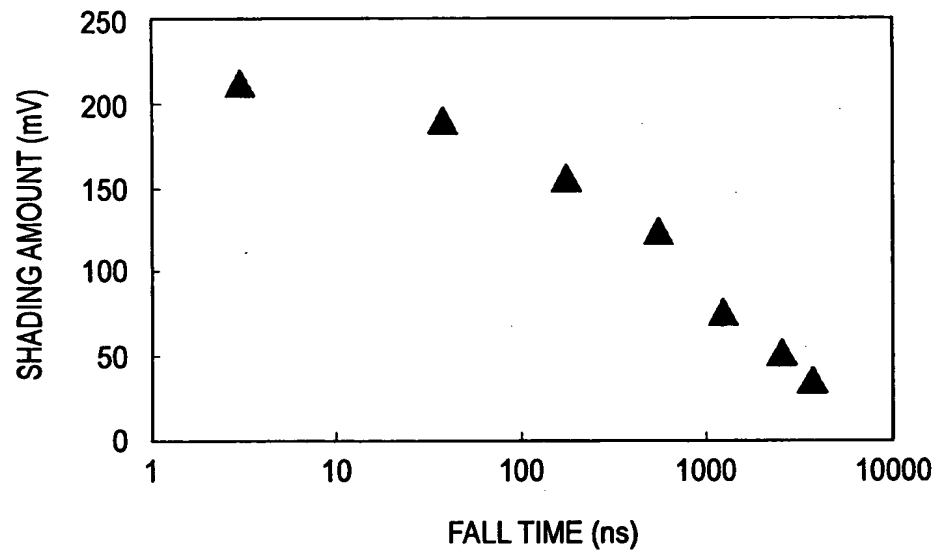
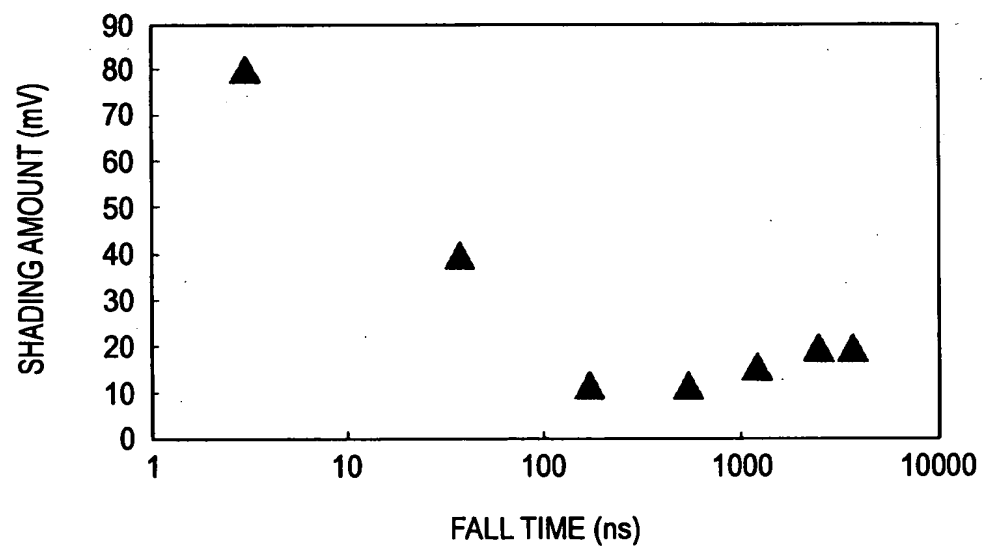
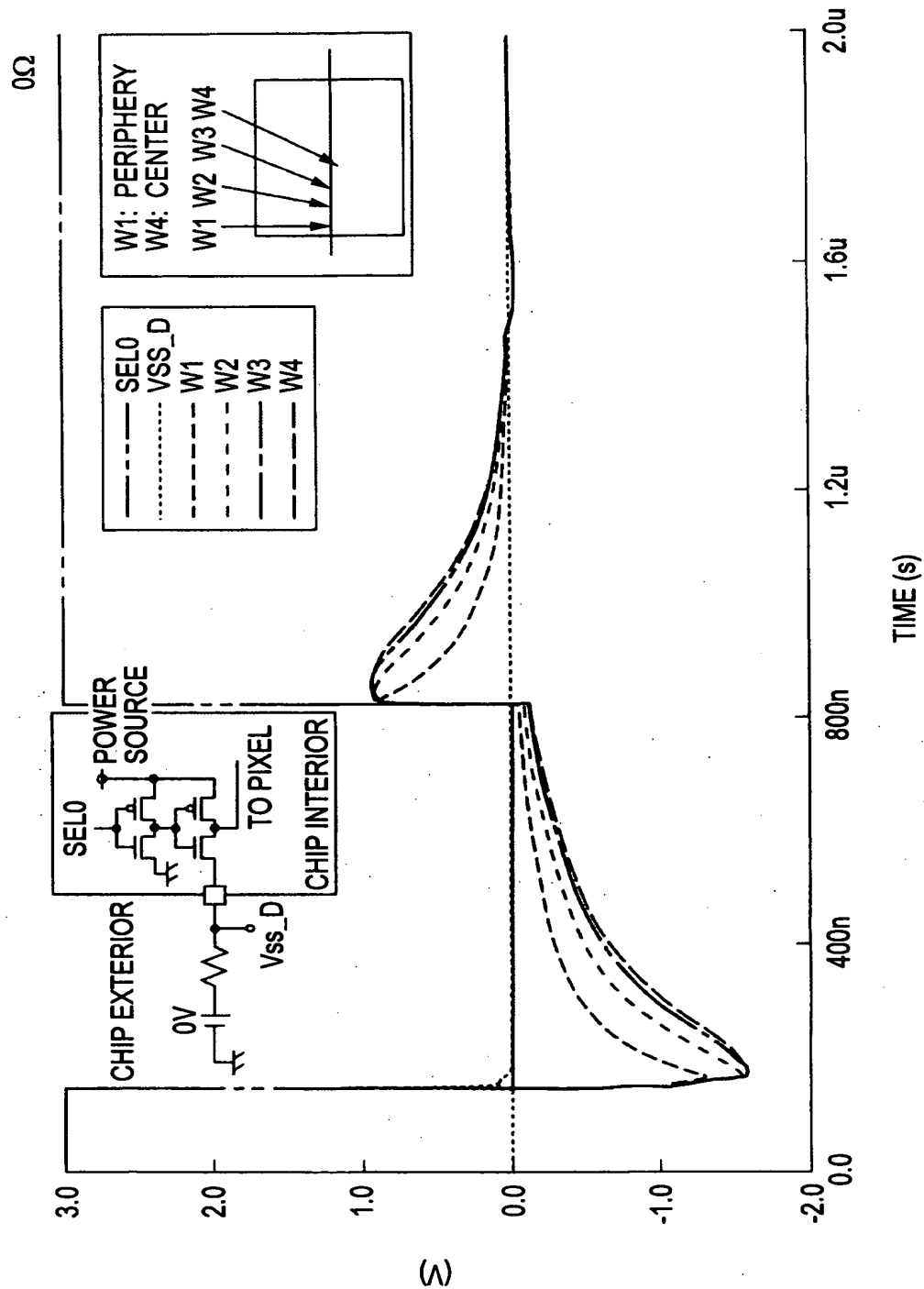
FIG. 5A**FIG. 5B**

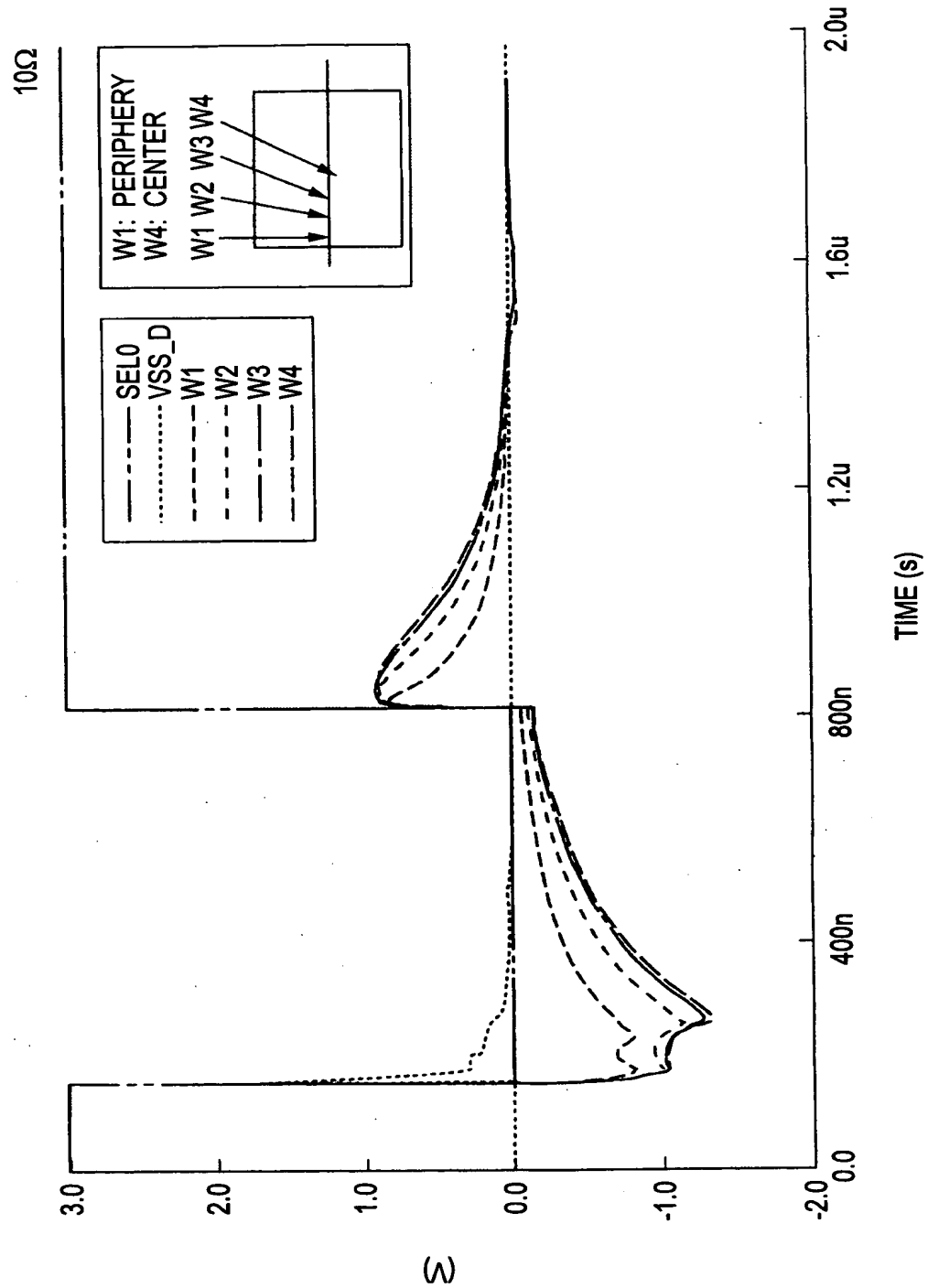
FIG. 6



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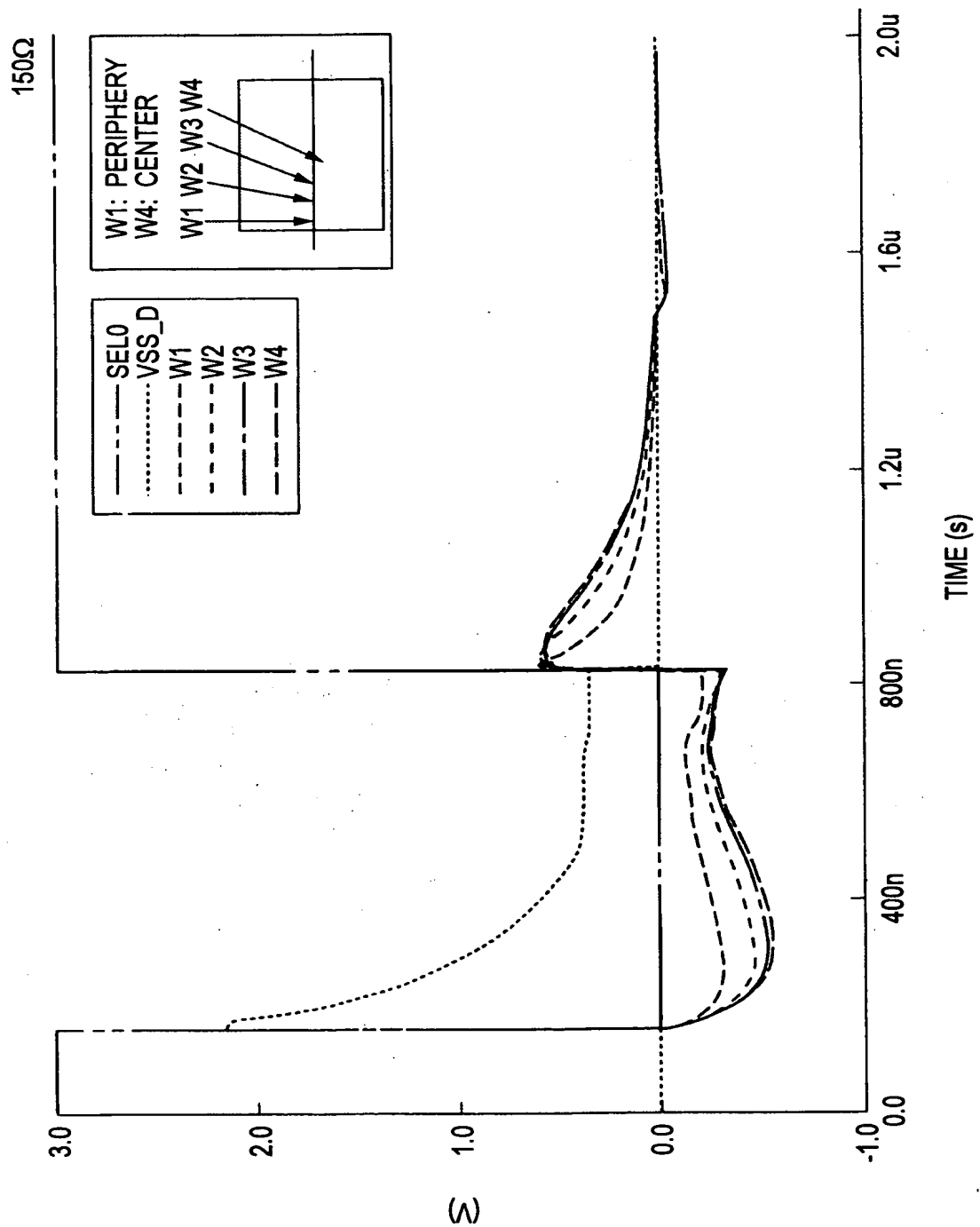
FIG. 7



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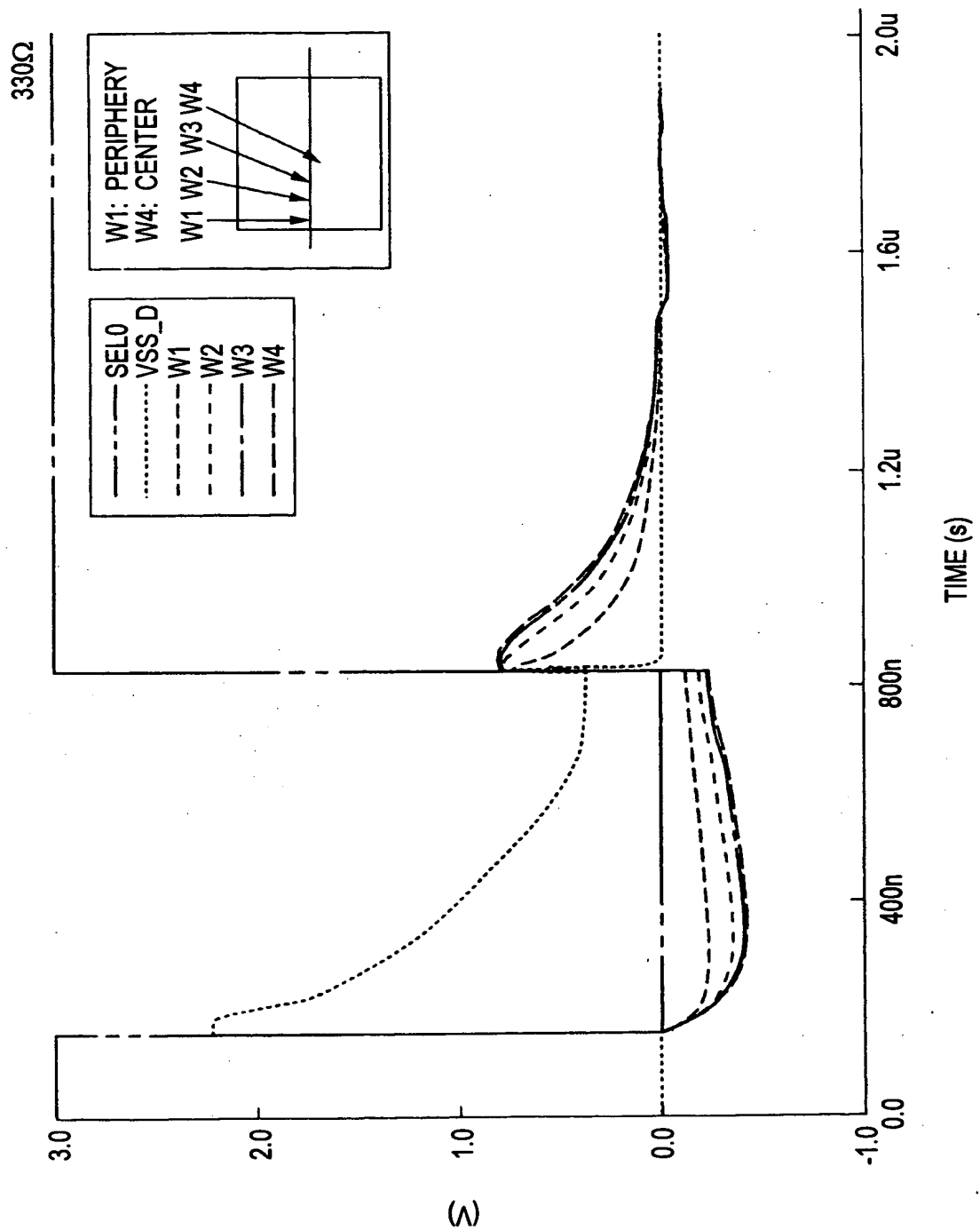
FIG. 8



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FIG. 9



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FIG. 10

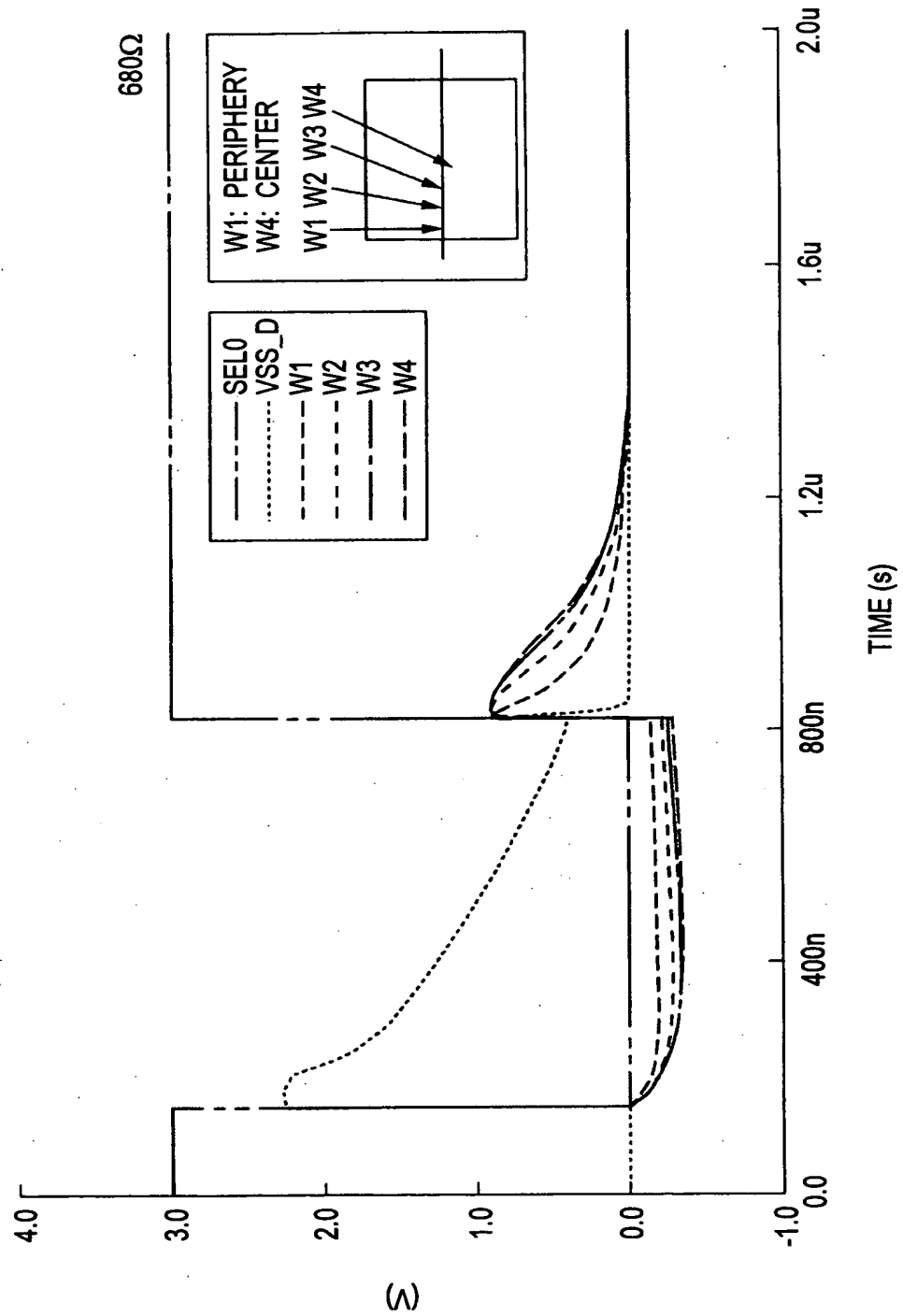


FIG. 11A

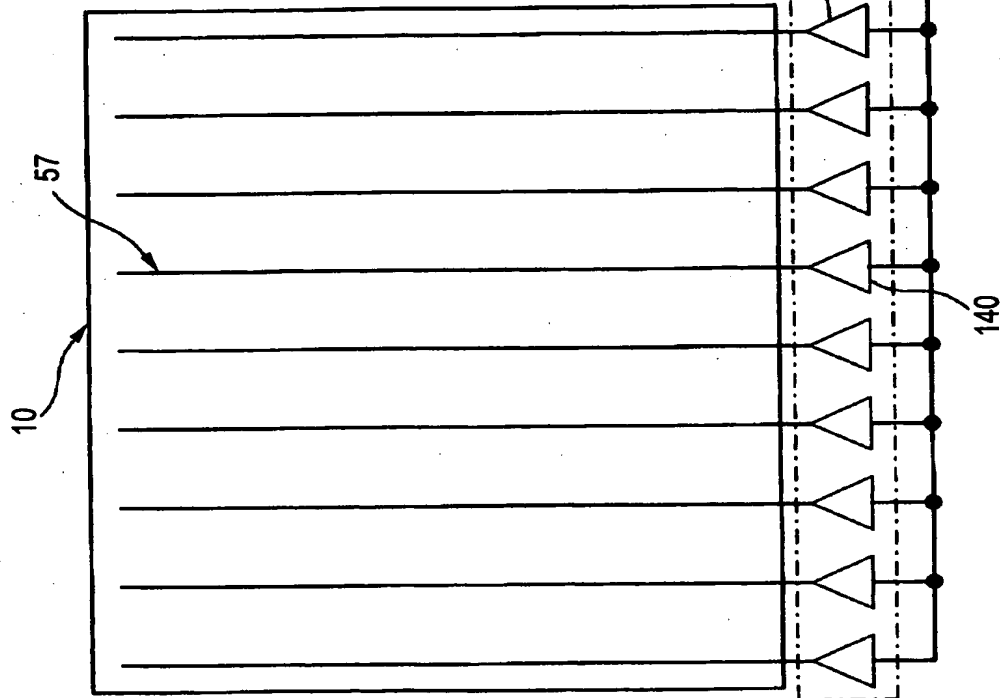


FIG. 11C

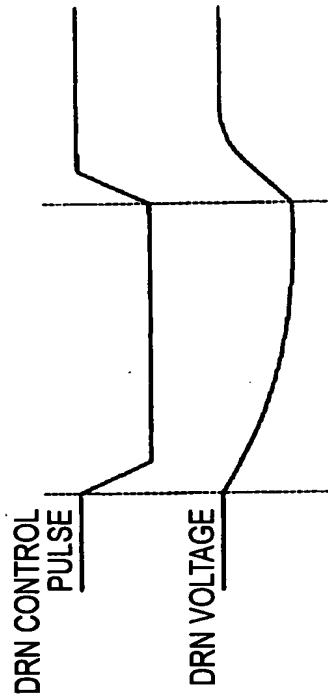
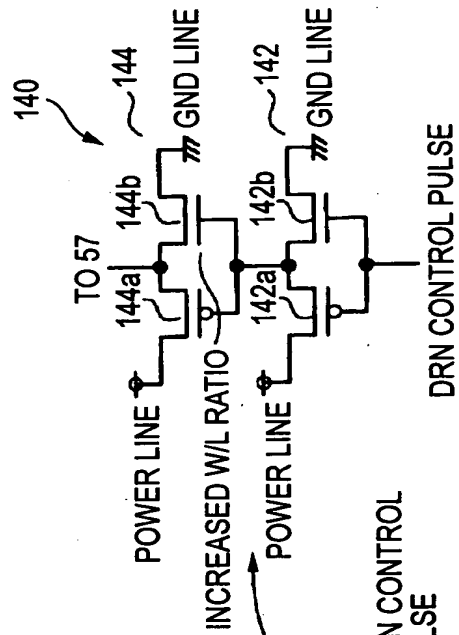


FIG. 11B



EXAMPLE OF BUFFER FINAL-STAGED NMOS W/L (FOR PIXEL-COUNT VGA CLASS)

	USUAL DESIGN (FALL OF SEVERAL ns OR LESS)	EMBODIMENT DESIGN (PRACTICAL VALUE AT FALL OF 40-10ns)
BUFFERS PRESENT ON EACH COLUMN	10/0.6	1/0.6-1/20 (USUAL RATIO 1/10 OR LESS)
BUFFERS PRESENT AT BOTH ENDS OF EACH ROW	6/0.6	1/1-1/20 (USUAL RATIO 1/10 OR LESS)
DRIVING DRN LINES ON THE PIXEL-REGION ENTIRE SURFACE BY ONE BUFFER	5000/0.6	500/0.6-2/20 (USUAL RATIO 1/10 OR LESS)

FIG. 12A

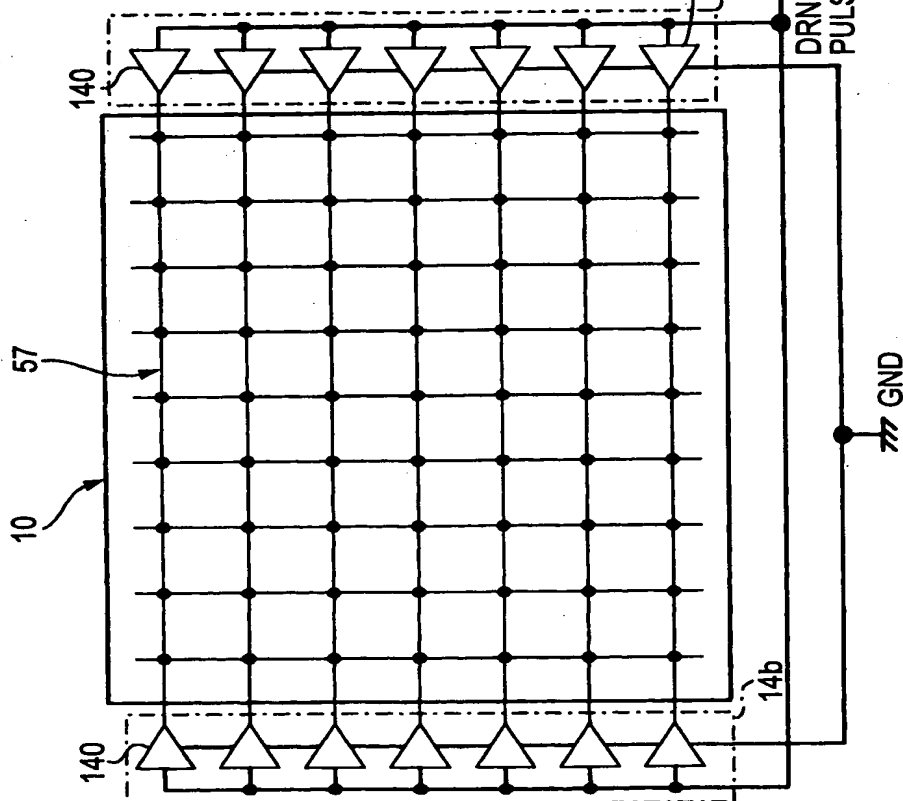


FIG. 12B

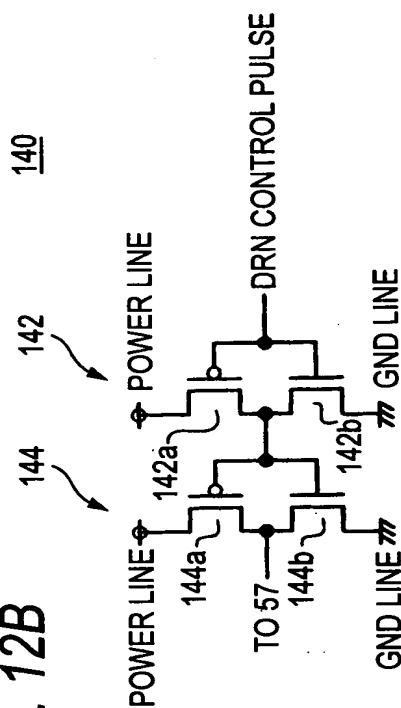


FIG. 13B

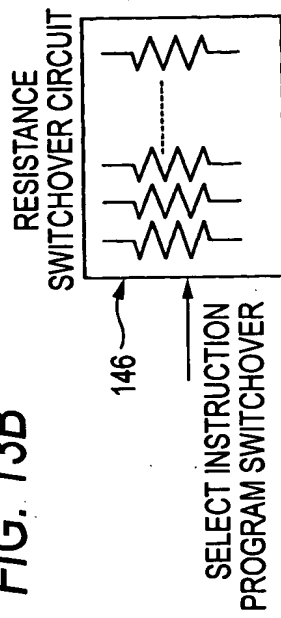


FIG. 13A

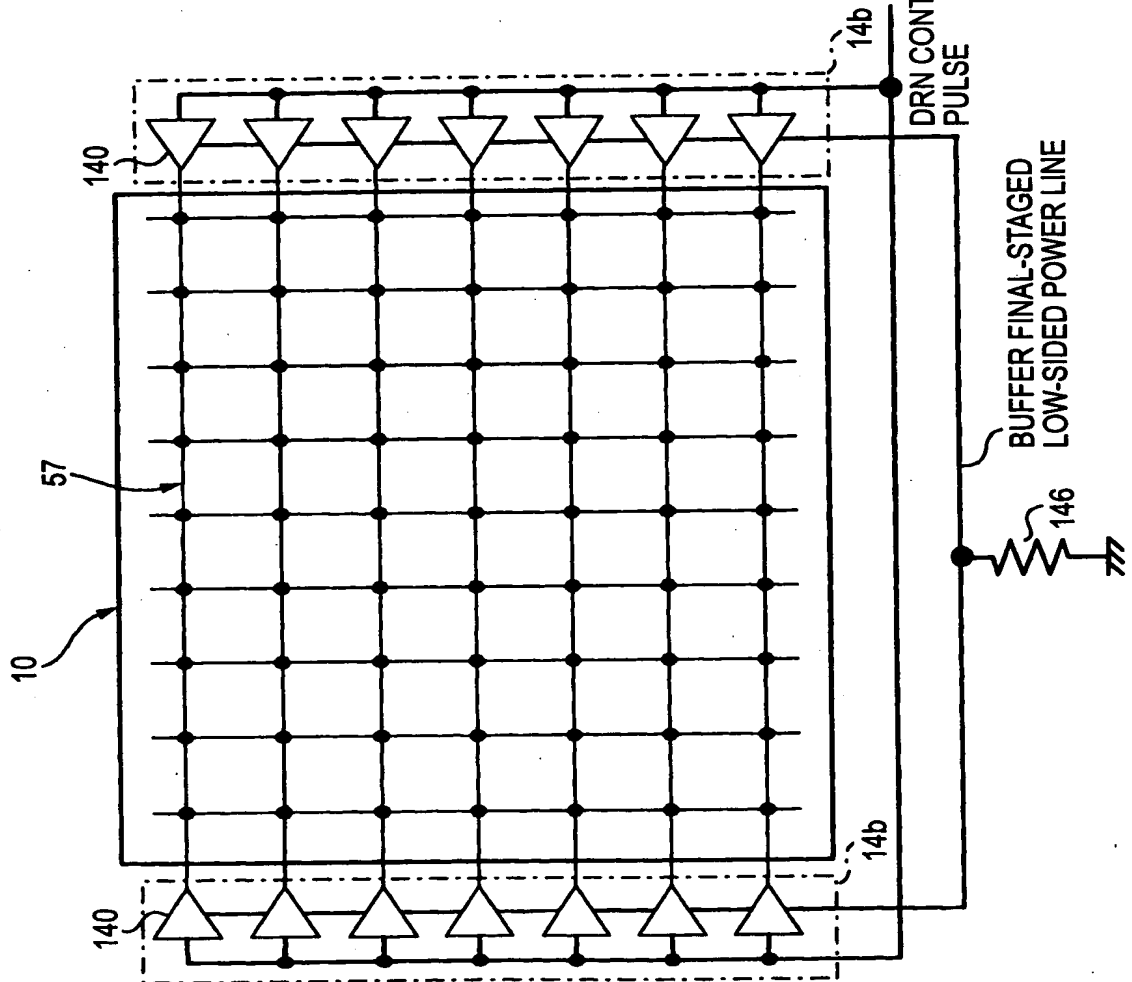
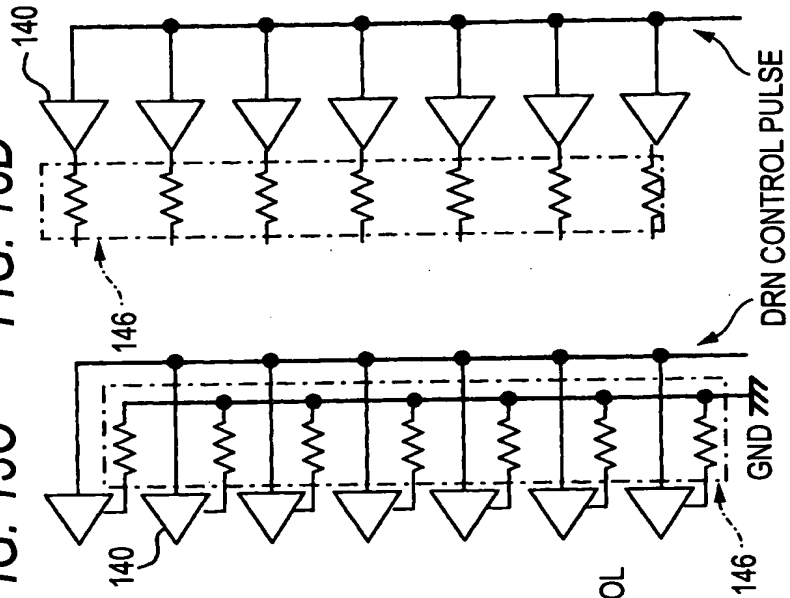


FIG. 13C



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FIG. 14A

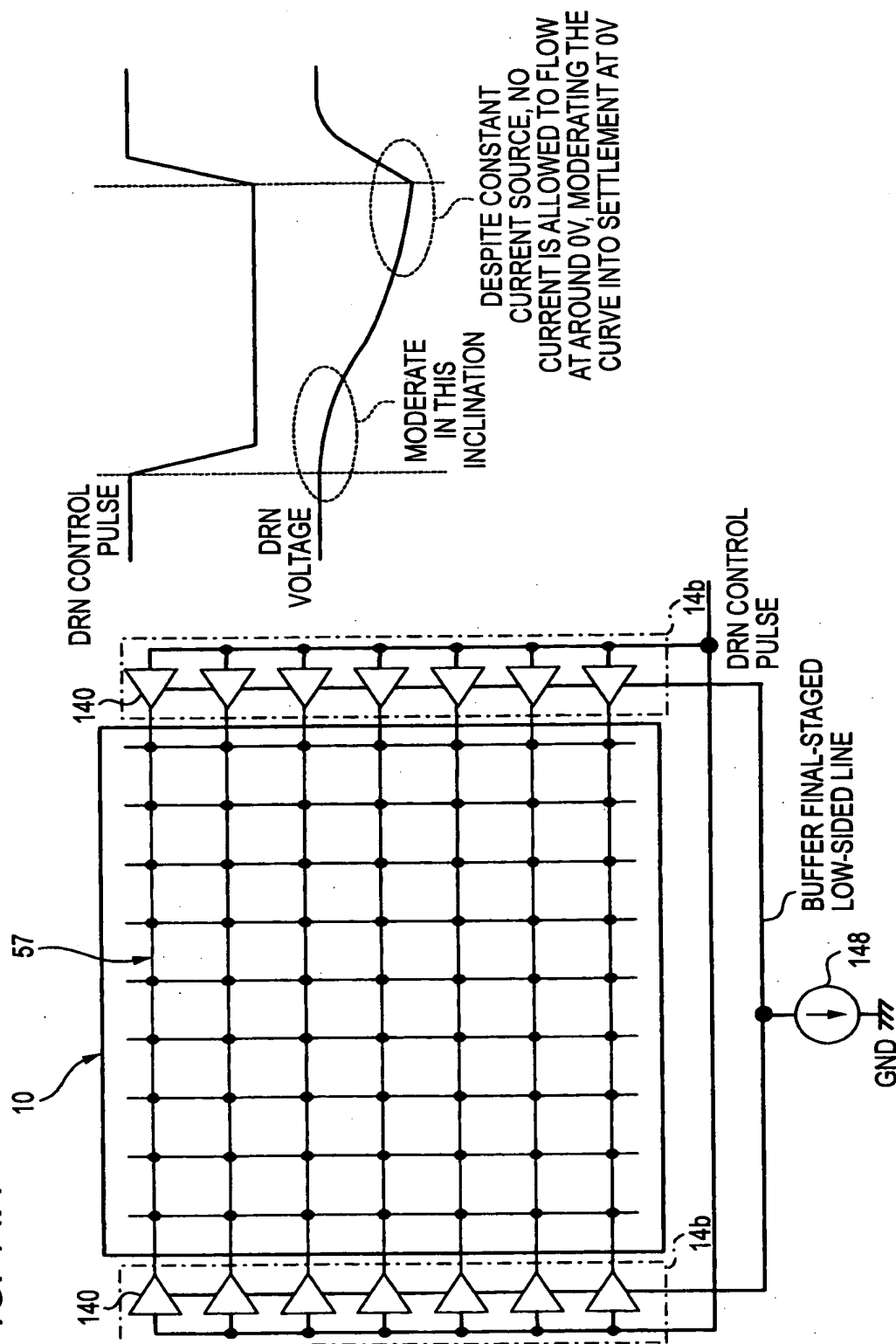


FIG. 15A

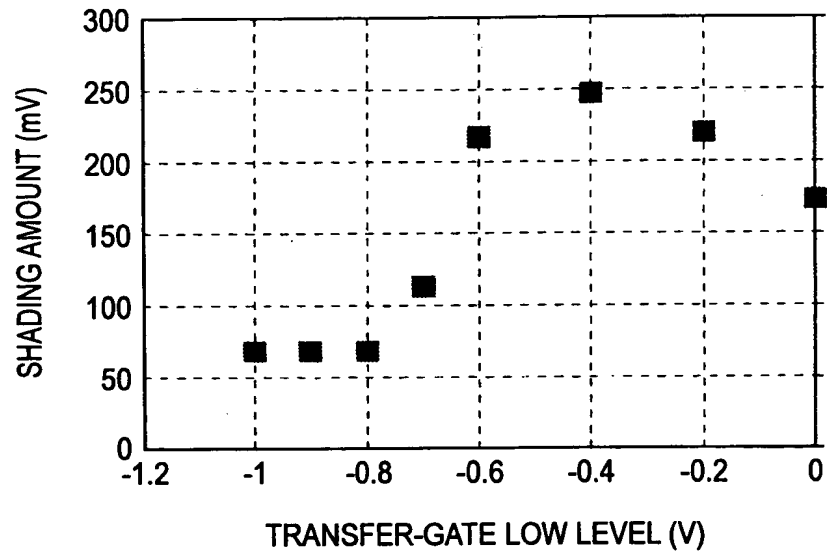


FIG. 15B

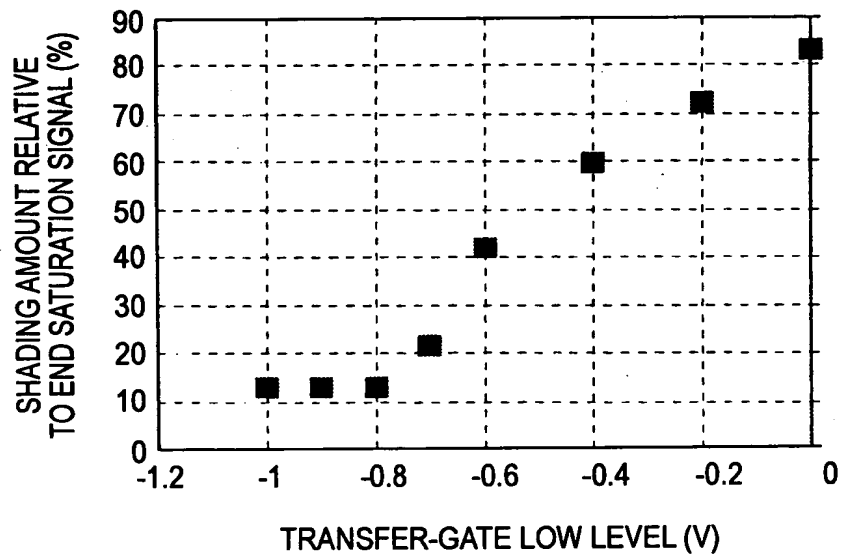


FIG. 16

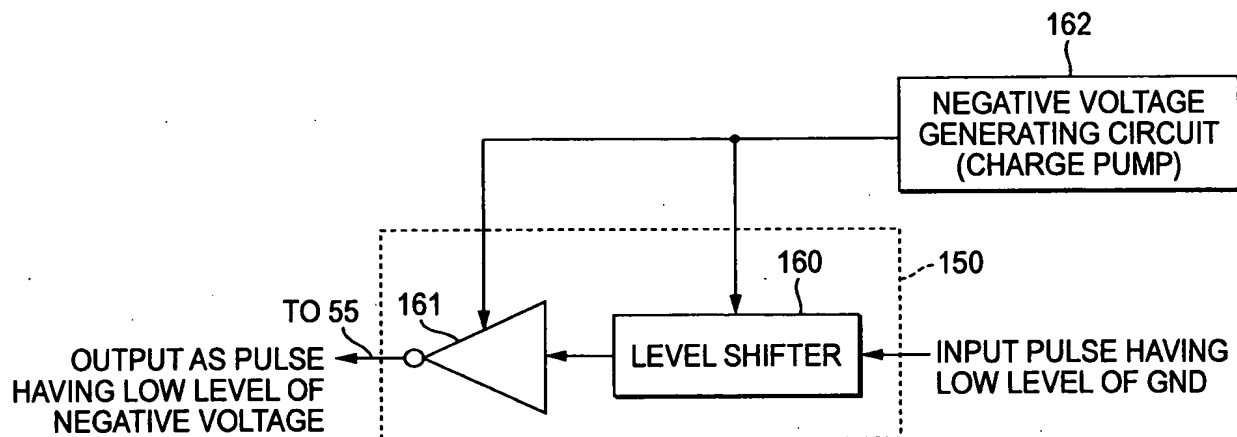


FIG. 17

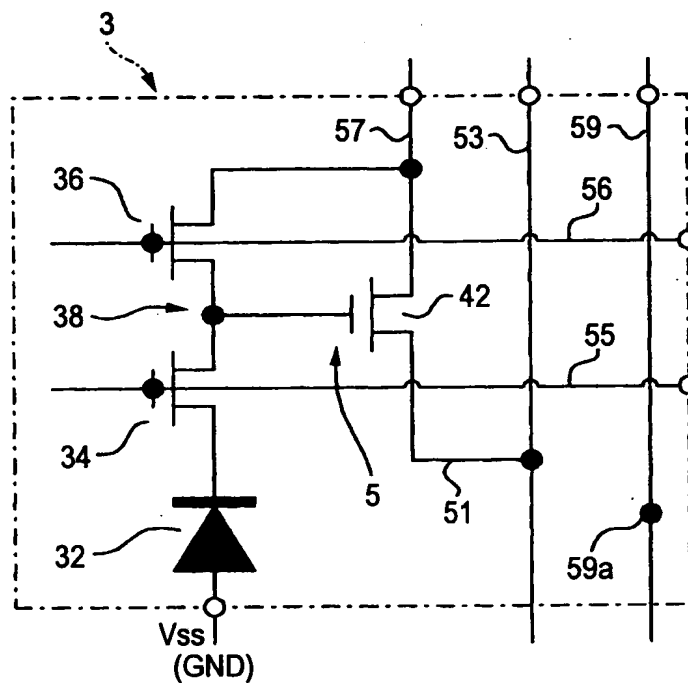


FIG. 18A

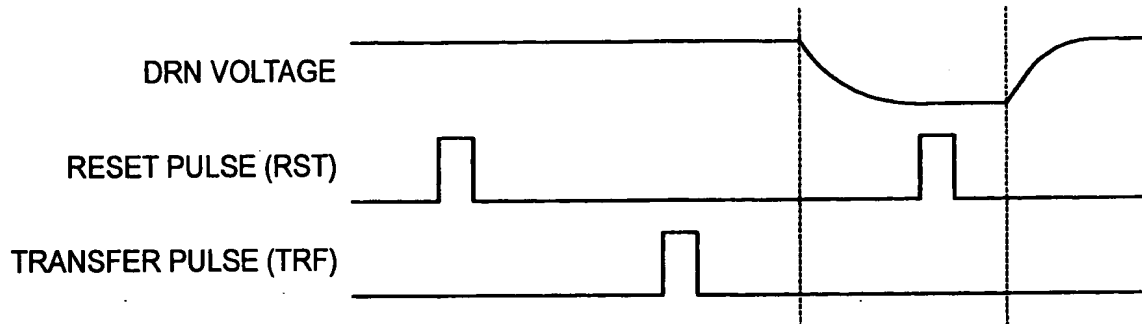


FIG. 18B

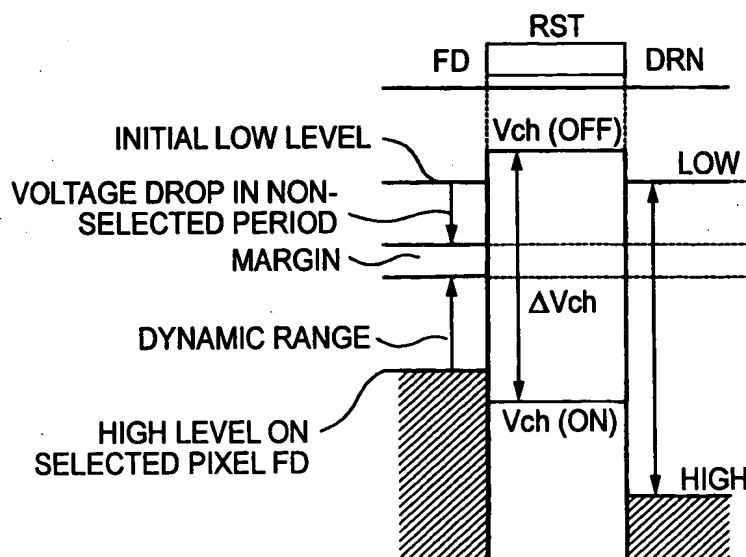
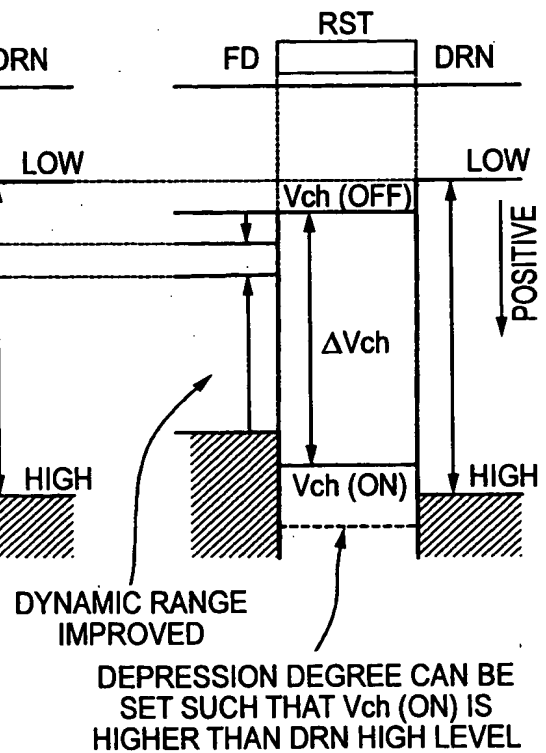


FIG. 18C



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[illegible]